URN etd-0407109-183710-798
Author Yong-Quan Lin
Author's Email Address No Public.
Statistics This thesis had been viewed 53 times. Download 134 times.
Department
Year 2005
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title Design of High-Fold Encoders
Date of Defense 0000-00-00
Page Count 97

Keyword
Interpolate
sputtering
encoder
32-fold time
phase-lag methods

Abstract
A high-performance motion system must rely on a high-resolution encoder to offer the speed and position signals, close the control loops, and show its excellent performance. However, the cost of an encoder is about half that of a motor rated below 1 hp. In order to reduce cost and raise the resolution, it is necessary to explore its internal circuit.
In the thesis, the relationship between sine and cosine functions is considered to obtain a four-fold frequency of the original by interpolating, and to utilize the phase-lag approach to raise it two times. In addition, the detection of rising and falling edges of channel A and channel B of an encoder is utilized to get the other four times in frequency. The algorithm to raise 32-fold times in frequency is implemented by two ways, hardware circuit or microcontroller-based circuit, in the thesis. Additionally, design on absolute encoders by sputtering thin film onto the disk is also studied. There generally exist variations of amplitude, phase, and DC level for the sinusoidal waveforms detected from the encoder. The thesis will discuss these issues and the compensation methods to get smooth waveforms by using FPGA/CPLD, ADC, and DAC. Finally, the algorithms and circuits will be applied to an optical encoder and a magnetic encoder to demonstrate their effectiveness.
Advisory Committee Ming-Shyan Wang - advisor

Files etd-0407109-183710-798-001.pdf
etd-0407109-183710-798-002.pdf

indicate access worldwide
Date of Submission 2006-08-03